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EXAMINER	
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ART UNIT	PAPER NUMBER
2624	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/749,694	GORINEVSKY, DIMITRY
	Examiner	**Art Unit**
	Nathan Bloom	2624

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/06/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Applicants' response to the last Office Action, filed on August 6th, 2007 has been entered and made of record.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 7, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biemond in further view of Nash ("VLSI Implementation of a Linear Systolic Array").

Instant claim 1: A method of deblurring an image, comprising the steps of: downloading a blurred image having pixels into a systolic array processor, said processor comprising an array of processing logic blocks in parallel such that groups of pixel arrive in respective processing logic blocks [*Biemond discloses an iterative method for image deblurring performed by a computing system. Biemond describes the method used to process the image but does not explicitly teach the downloading of the image or the use of a systolic array processor to perform the deblurring method. Examiner takes official notice that the downloading of the image for processing is notoriously well known in the art, and is in fact an intrinsic step of an image processing method that augments an existing image. Nash teaches the use of a systolic array for linear processing, and in the 2nd paragraph on page 1 that the systolic array is broken*

down into processing elements (processing logic blocks). It would have been obvious to one of ordinary skill in the art to combine the teaching of Nash and Biemond to increase the processing performance of the system as is disclosed by Nash in the abstract. Furthermore, deblurring of images is disclosed as an application of the systolic array for on page 3 of Nash under the section entitled "Applications" and as further evidenced by Owens ("Computer Vision of the MGAP") in section 3.1 that the use of systolic algorithms (such as deblurring) for computer vision on an array processor (array processors perform parallel processing) was known to one of ordinary skill in the art.];

sequentially exchanging data between processing logic blocks by interconnecting each processing logic block with a predefined number of the processing logic blocks adjacent thereto [*Nash discloses in the section entitled "Linear Array Organization" the interconnection of the processing elements. Also, further arrangements of processing element interconnections were known as is evidenced by Amin ("PVM Implementations for Low-Level Image Processing Systolic Array Designs"). Furthermore, a systolic array processor such as is taught by Nash (see paragraphs 5 and 6 of page 1393) is used to concurrently (i.e. in parallel) perform similar operations and then shift this processed data to a next set of processing elements (data processing units, CPUs, ..., etc...) wherein a next linear manipulation is performed on the data.*];

and uploading the deblurred image [*Nash and Biemond do not explicitly teach the uploading of the blurred image. Examiner takes official notice that the uploading of the deblurred (processed) image is notoriously well known in the art. Since the purpose of deblurring the image is to produce a deblurred image for display or further processing, and thus it would have*

been obvious to one of ordinary skill in the art to store or upload the processed image for retrieval or display.].

Instant claims 7 and 14 claim the corresponding device that performs the method of instant claim 1. As per rejection of instant claim 1 the device has been disclosed.

3. Claims 5, 12, and 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Biemond and Nash in view of Owens ("Computer Vision of the MGAP").

Instant claim 5: The <u>method</u> of claim 1, wherein said processor groups pixel in groups that comprise at least one pixel. [*Biemond and Nash teach the deblurring of an image using a systolic processor but do not discuss in detail how the pixels are grouped for processing. Owens teaches the implementation of image processing methods using systolic array processors for image processing and in the final line of the 2nd paragraph on page 338 that at a least one pixel is operated on per processor. Thus, as is evidenced by Owens one of ordinary skill in the art would have understood how to group the pixels for processing. It would have been obvious to one of ordinary skill in the art to combine Biemond and Nash with Owens to implement the image processing applications as were suggested by Nash.*]

Instant claims 12 and 19 claim the corresponding device that performs the method of instant claim 5. As per the rejection of instant claim 5 the device has been disclosed.

4. Claims 2, 8, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nash in view of Biemond ("Iterative Methods for Image Deblurring") and Jagadish ("Array Architectures for Iterative Algorithms").

Instant claim 2: The method of claim 1, wherein said processing logic blocks providing an iterative update of said blurred image by (i) providing feedback of the blurred image prediction error using the deblurred image and (ii) providing feedback of the past deblurred image estimate [*Nash discloses the use of a systolic array for image deblurring as is disclosed in rejection of instant claim 1, but does not disclose the particular method. Biemond discloses an iterative method for deblurring images in pages 865-868 under the section titled "C. Iterative Solutions". In particular, see equations 56 and 57 on page 865. Furthermore, as is evidenced by Jagadish in sections 3-5 the implementation of iterative algorithms on a processing array were well known to one of ordinary skill in the art. In particular section 3 of Jagadish discloses the procedure of obtaining the array architectures for iterative algorithms, section 4 shows examples, and section 5 discusses irregular cases. It would have been obvious to one of ordinary skill in the art to combine Nash and Biemond given that it was known in the art to solve image deblurring using iterative methods (as taught by Biemond), and that it was known to use high performance processing arrays for deblurring (as taught by Nash) at the time of the invention. See the Abstract and Applications sections of Nash for the suggestion of using these high performance, low complexity processing arrays for image deblurring.*]

Instant claims 8 and 15 claim the device corresponding to the method of instant claim 2. As per rejection of instant claim 2 the device has been disclosed.

5. Claims 3, 9-10, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nash in view of Biemond, Jagadish, and Gorinevsky ("Optimization-based Tuning of Low-bandwidth Control in Spatially Distributed Systems").

Instant claim 3: The method of claim **2**, wherein said iterative update is implemented in said processing logic blocks by $u(n+1) \equiv u(n) - K * (H * u(n) - y_b) - S * u(n)$ [*Biemond: see equations 56 and 57 on page 865, u(n+1)=f(k+1), u(n)=f(k), g=* y_b , *K=B, and H=H*] where u is the ideal undistorted image, m and n are column and row indices of an image pixel element, $y_b(m,n)$ is the observed blurred image, * denotes a 2-D convolution, K is a feedback update operator with a convolution kernel k(m,n) and S is a smoothing operator with a convolution kernel s(m,n) [*Biemond identifies the existence of regularization error and discloses a solution of the regularization error in section 5 which begins on page 868. The term* $S * u(n)$ *as defined by applicant was known to one of ordinary skill in the art as a solution to the regularization problem. Biemond does not teach the regularization method shown by applicant. However, Gorinevsky in sections 1 and 3 teaches a filter that improves the spatial response (reduces regularization error) of the system. It would have been obvious to one of ordinary skill in the art to substitute the regularization method as taught by Gorinevsky for the regularization method taught by Biemond with a reasonable expectation of success while maintaining or improving the*

spatial response (reduction of regularization error) provided by the method taught by Biemond. Furthermore, in the same sections of Gorinevsky the use of the term K has also been disclosed.].

Instant claims 9 and 16 claim the device corresponding to the method of instant claim 3. As per rejection of instant claim 3 the device has been disclosed.

Instant claims 10 and 17: The device of claim 9 [*and 16*], wherein the operators H, K, and S are preloaded in each of the array processing logic blocks. [*Nash, Jagadish, and Gorinevsky do not explicitly teach the preloading of the information into each processing logic block. However, Examiner takes official notices that it is notoriously known that in order to perform mathematical computations with these operators that the these factors would have to have been initialized prior to performing the computations.*]

6. Claims 4, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nash in view of Biemond, Jagadish, and Gorinevsky ("Optimization-based Tuning of Low-bandwidth Control in Spatially Distributed Systems") as applied to claims 3, 9-10, and 16-17 in further view of Dowski (US 2003/0169944).

The method of instant claim 4 is a modification of the method of instant claim 3 wherein the deblurring is performed on each color space separately. Biemond, Jagadish, and Gorinevsky discuss image processing, but do not go into the particulars of color space processing. However, as is evidenced by Dowski in paragraph 0018 the method of dividing an image into its color

spaces and then deblurring each of the color spaces was known to one of ordinary skill in the art. The teaching of Dowski shows that one of ordinary skill in the art knew how to apply image-filtering processes such as deblurring to each color channel. Given that Biemond at least teaches the deblurring of a grayscale image and that Dowski teaches the application of a single channel deblurring process to each of the color channels. Then it would have been obvious to one of ordinary skill in the art to combine the teachings of Dowski with Biemond to perform the deblurring technique as taught by Biemond on each channel of a color image and yield the expected result of a deblurred color image.

Instant claims 11 and 18 claim the device corresponding to the method of claim 4. As per the rejection of instant claim 4 the device has been disclosed.

7. Claims 6, 13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nash in further view of Owens ("Computer Vision on the MGAP").

Instant claim 6: The method of claim 5, wherein said groups of pixels comprises a group selected from 2 by 2 pixels, 3 by 3 pixels, and 4 by 4 pixels. [*Filtering and image processing methods such as deblurring are done locally by particular filter sizes depending on the desired outcome. Owens describes image processing using array processors is section 3.1 on page 338 disclosed the use of 3x3 masks applied to the image and hence it was known to group and process pixels in the 3x3 format in a processing array. It would have been obvious to one of*

ordinary skill in the art to combine Nash and Owens to improve the utility and efficiency of the processing arrays by allowing local filtering operations to be performed on groups of pixels.]

Instant claims 13 and 20 claim the device corresponding to the method of instant claim 6. As per the rejection of instant claim 6 the device has been disclosed.

Response to Amendment

The amendments to claims 3-4, 9, and 11 overcome the 35 USC 112 2nd paragraph rejection for lack of antecedent basis. Furthermore, the amendment to claim 5 overcomes the minor informality objection.. Thus, the 35 USC 112 2nd paragraph rejection for lack of antecedent basis of claims 3-4, 9, and 11 and the objection to claim 5 have been withdrawn.

Response to Arguments

8. Applicant's arguments filed on August 6th, 2007 have been fully considered but they are not persuasive.

With regards to the 35 USC 103 rejection of claims 1, 7, and 14 applicant argues:

Applicants' argue that it is not well known to download an image for processing or to upload a processed image. Examiner maintains the official notice that it was notoriously well known to one of ordinary skill in the art to download an image to an image-processing device. If an image was not downloaded into such a device then the method that it performs on the image would not occur thus it is inherent that any image-processing device that acts upon an existing image must first obtain that image by downloading it in a known manner. Furthermore, the examiner

maintains that uploading an image after processing was notoriously well known to one of ordinary skill in the art. If this was not the case then the image data would not be stored or displayed, but would just be processed then deleted. However, this is not the case as it was common practice at the time of the invention to output the image data to a storage or display device.

Applicants' argue that Biemond does not disclose logic blocks or the sequential exchange of data between interconnected adjusted processing logic blocks, and thus that there is no disclosure that the groups of pixels arrive in processing logic blocks. Examiner relies on Biemond's teachings of an iterative image deblurring method and not for the teachings of using the processing logic blocks of a systolic array processor to perform the method taught by Biemond. Nash is relied upon for teaching the use of a linear systolic array processor for image processing.

"*Nash Is cited for teaching that the systolic array is broken into processing elements (the language of Nash) which the Examiner then equates as processing logic blocks. However, there is no suggestion in Nash (or the other references) that processing elements are processing logic blocks as called for by the instant clai9ms. Further, the Examiner has taken the phrase "image restoration" that is briefly noted in Nash to imply that Nash is adaptable to deblurring. That is not disclosed. More importantly, Nash is concerned with a linear systolic array. It is not capable of performing computations that "are however, performed in parallel by the processing logic blocks of the array." (Page 11, lines 13-14 of this application as filed). The independent claims have been amended to more clearly describe this parallel calculation.*"

Applicant is merely stating that the "processing elements" as described by Nash are not the same as the "processing logic blocks" described by the applicant, but provides no evidence or

explanation as to what differs between these components and thus does not meet the requirements of 37 CFR 1.111. Furthermore, Nash in line 11 of the "Applications" section clearly states that image deblurring is one of the methods that can be performed by the linear systolic array processor. Also, the argument that Nash does not teach a parallel processing technique/apparatus is unsubstantiated as Nash clearly teaches a systolic array which by definition is inherently a parallel processing device. Examiner takes official notice that it was common knowledge to one of ordinary skill in the art that a systolic array processor is a grid (or array) of processing elements that perform predetermined operations in parallel.

Applicants' argue that Biemond in view of Nash do not meet the first criteria of MPEP 2142, but do not explain why the motivation to combine these teachings as shown by examiner is insufficient. Examiner would like to point out that the motivation is stated within the previously and currently presented 35 USC 103 rejection. Biemond teaches the iterative image deblurring method and Nash teaches in the "Abstract" section that systolic array processing is flexible and high performance processing and in the "Applications" section wherein Nash suggests that image deblurring would benefit from the processing device and method.

With regards to the 35 USC 103 rejections of claims 5, 12, and 19 applicant argues:

"The Examiner concedes that Biemond and Nash do not discuss how the pixels are grouped for processing, and has cited Owen to show that a single pixel is operated on per processor. While that may be true, it does not remedy the deficiency of the primary references that do not disclose parallel calculations with adjacent processing logic blocks."

As per the 35 USC 103 rejections of these claims Biemond and Nash do not discuss how the pixels are grouped. However, when processing an image via even a single processor the pixels must be organized or grouped accordingly for the processor to operate on the given data in a known and predetermined manner. This manner is not explicitly stated in most image processing methods, as one of ordinary skill in the art knows how to group the pixels for processing the image. The teaching of Owens was relied upon merely to evidence that one of ordinary skill in the art understood how to process images (arrays of pixels) using systolic array processors. Owens does not explicitly state the grouping of the pixels for image processing, but shows that it was known to use systolic array processors for image processing. Furthermore, one of ordinary skill in the art recognizes that the array of processors will not perform any image processing unless the image data is broken down into groups of pixels and then operated on by the array of processors.

With regards to the 35 USC 103 rejections of claims 2, 6, 8, 13, 15,and 20 applicant argues:

"This last reference is cited as teaching the "implementation of iterative algorithms on a processing array." Once again the combination doe not disclose or suggest parallel calculations with adjacent processing logic blocks. Withdrawal of the rejection is requested"

"As has been demonstrated above, Nash does not teach parallel calculations and Owen does not remedy that deficiency."

Please see the prior discussion of the previously presented argument that "Biemond in view of Nash do not teach the parallel processing using logic blocks".

With regards to the 35 USC 103 rejections of claims 3-4, 9-11, and 16-18 applicant argues:

"This latter reference relates to mathematical calculations but in no way looks at image deblurring and has been cited based only on Applicant's disclosure and not in accordance with MPEP 2142. The Examiner has made reference to Dowski (US 2003/169944) but that reference was not listed on the Notice of References cited. Nevertheless, Dowski does not remedy the deficiencies of the other references simply by dividing an image into color spaces and does not teach deblurring. "Further processing" does not teach deblurring. Withdrawal of the rejection is urged."

Examiner has adjusted the rejection of claim 3 such that the use of Gorinevsky in view of the other teachings is clear. Biemond teaches a solution to the regularization problem and the reason that regularization is necessary, but does not teach Applicants' particular method of carrying it out. Gorinevsky is relied upon to show that the regularization solution taught by Applicants was known. Furthermore, the substitution of Gorinevsky's solution for that of Biemond's would've been obvious to one of ordinary skill in the art as they are alternative solutions to the same problem and there is a likelihood of success in implementing Gorinevsky's solution for that of Biemond's. Examiner relied on Dowski to show that the processing of color images by division of the data into color spaces in order for further image processing to be performed on each color space was known to one of ordinary skill in the art. Applicants' argument that the "further processing" is not image deblurring and that Dowski does not teach image deblurring is irrelevant since Gorinevsky is not relied upon for these teachings. Furthermore, Examiner has restructured the rejection in view of Dowski to more completely convey Examiner's point and included the Dowski reference in the "References Cited" form.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan Bloom whose telephone number is 571-272-9321. The examiner can normally be reached on Monday through Friday from 8:30 am to 5:00 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Samir Ahmed, can be reached on 571-272-7413. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

SAMIR AHMED
SUPERVISORY PATENT EXAMINER